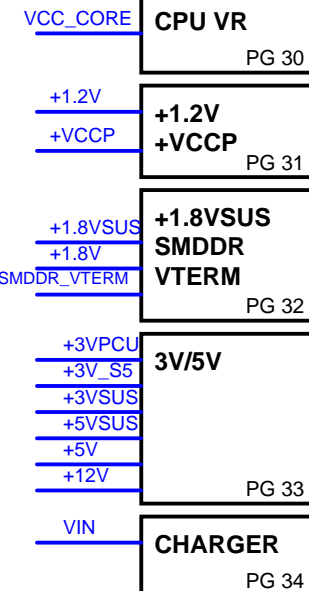


BOM MARK
SA@ SATA 要打
PA@ PATA 要打
3@ 3G 要打

ZH3

ZH3 ASSY P/N :31ZH3MB0008
ZH3 MB C/S ASSY P/N: 41ZH3CS0001
ZH3 MB S/S ASSY P/N: 51ZH3SS0003



DDRII-SODIMM1 PG 7,8

DDRII-SODIMM2 PG 7,8

AMD S1
Turion 64 Rev.F Dual-Core/
Sempron Rev.F Single-Core
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
PG 3,4,5,6

CPU THERMAL
SENSOR
Page 5

DVI
TI TFP513PAP
Page : 29

DVI

Docking
Page : 30

EXT CRT

DVO

TVOUT

RGB

LVDS

CRT Switch
SN74CBTLV3257PWR
Page : 16

INT CRT

CRT
Page : 16

LVDS
Page : 16

Mini Card (WLAN) PCIE3 & USB4
PCI Express Mini Card PG 19

PCI-E, 1X

Express Card PCIE2 & USB5
NEW CARD PG 31

PCI-E, 1X

USB 2.0 * 1(USB5)

RS485
465 FCBGA
PG 9,10,11,12

A_LINK

SATA - HDD PG 23

SATA0

PATA - HDD PG 23

PATA 100

SB460
549 BGA
PG 14,15,16,17

USB2.0 (P0~P7)

Bluetooth
USB7 PG 20

USB2.0 I/O Port X3
USB0 & USB1 & USB2 PG 20

DSC USB I/F
USB6 PG 16

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz

CLOCK GENERATOR
ICS951462
PG 2

REF 14MHz

PCI Bus 33MHz

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7412	AD25	REQ0# / GNT0#	INT E/F/G#
5788M	AD20	REQ2# / GNT2#	INT G#

AD25
REQ0# / GNT0#
INT E/F/G#

OSC
48MHZ

BROADCOM
10/100/1G LAN
5788M PG 17

BOTH HAND
TRANSFORMER PG 18

RJ45
PG 18

Azalia Audio
PG 24

Amplifier
MAX4411 PG 25

Amplifier
MAX9755A PG 25

Azalia MDC
PG 24

MIC.
PG 25

H.P/SPDIF
PG 25

INT.
S.P.
PG 25

MODEM
RJ 11
PG 18

G-SENSOR
KXP84-0200
Page : 23

KBC
NS97551
PG 27

NS
SIO (87383)
Page : 26

K/B
CONN.
PG 28

Touch
Pad
PG 28

Flash
ROM
PG 27

FIR
Page : 26

X-Bus

TI
PCMCIA+1394
+6 IN 1
PCI7412
Page : 21~22

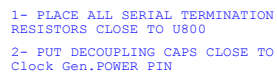
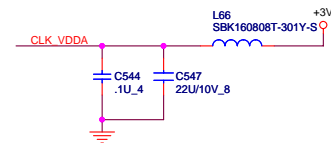
1394
Page: 21

5 IN 1
Page: 22

PCMCIA
Page: 22

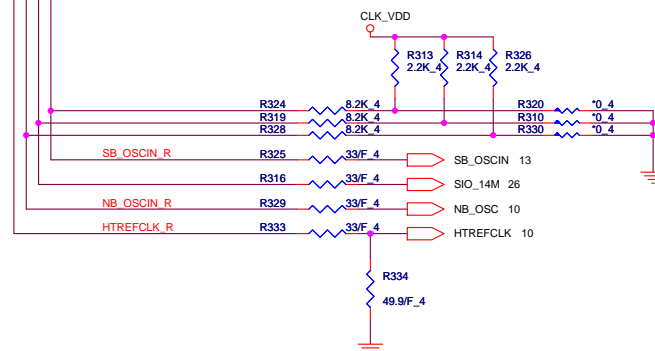
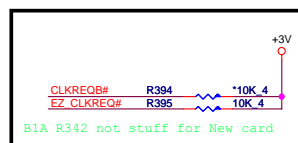


PROJECT :ZH3
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FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

```
CLKREQA# Controls SRC5,6,7
CLKREQB# Controls SRC2,3,4,ATIG3
CLKREOC# Controls SRC0,1,ATIG0,1,2
```





PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

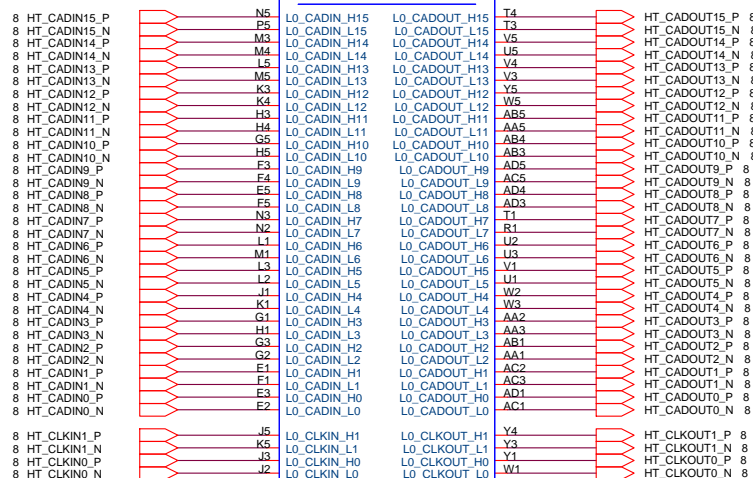
VLDT_RUN U20A

D4 VLDT_A3
D3 VLDT_A2
D2 VLDT_A1
D1 VLDT_A0

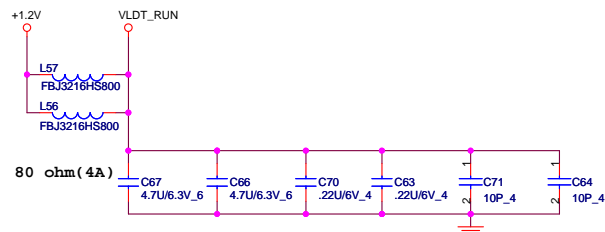
VLDT_B3
VLDT_B2
VLDT_B1
VLDT_B0

AE5
AE4
AE3
AE2

C69 4.7U/6.3V_6



Athlon 64 S1
Processor Socket



LAYOUT: Place bypass cap on topside of board

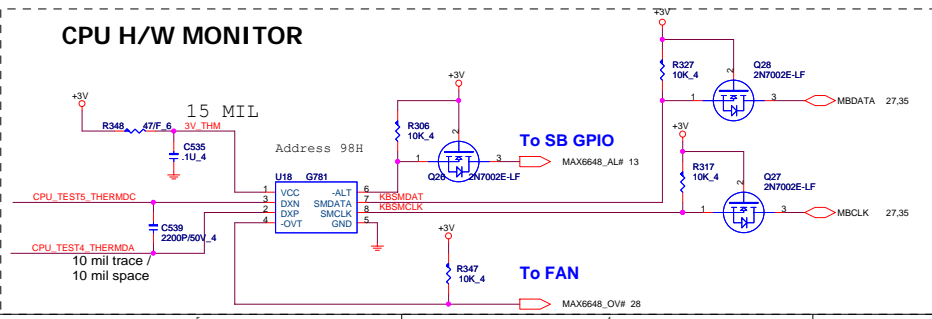
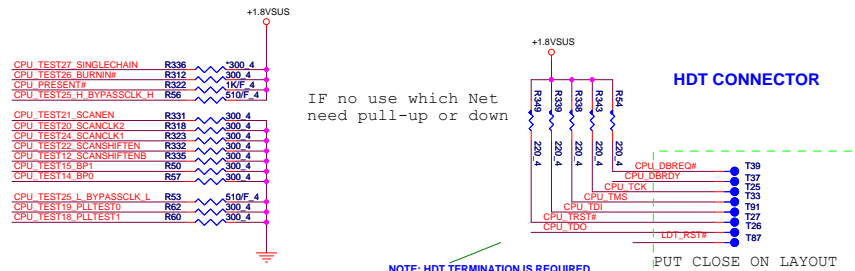
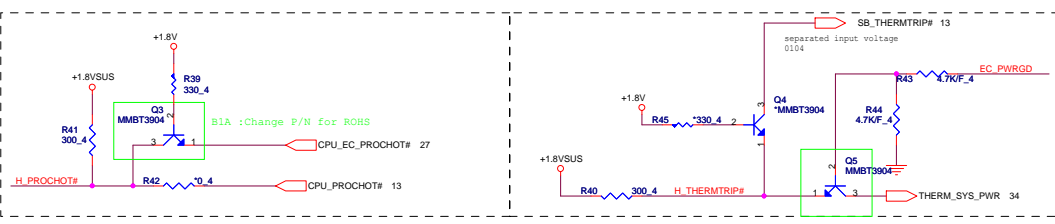
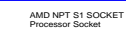
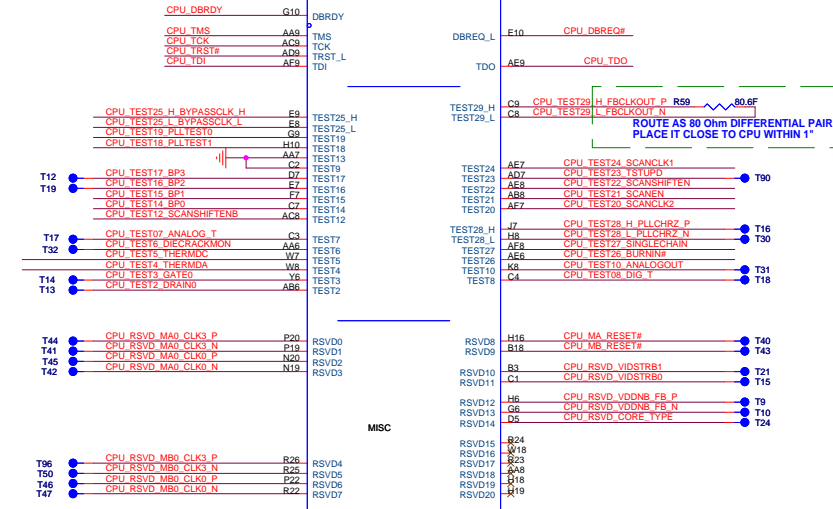
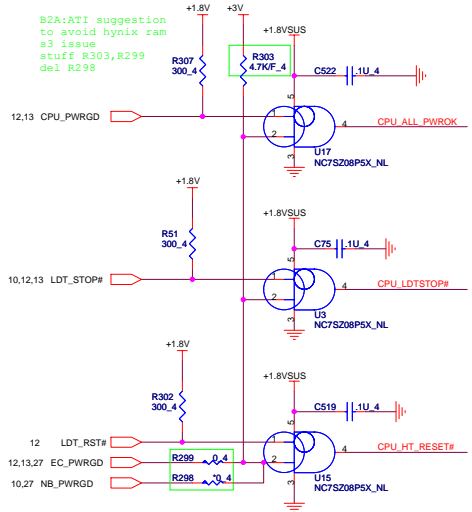
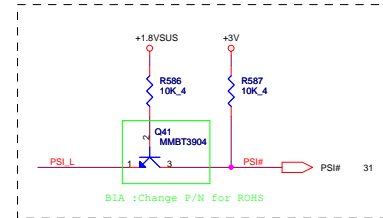
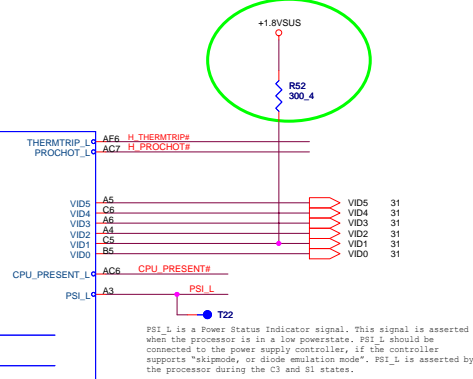
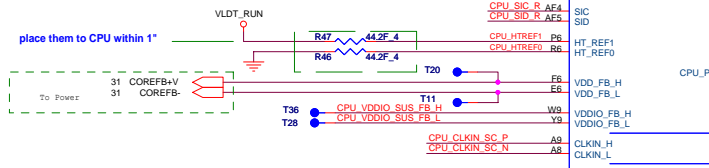
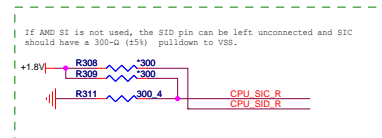
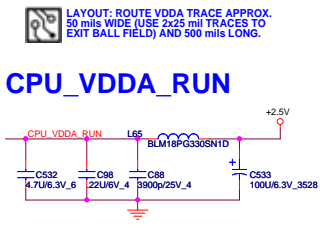


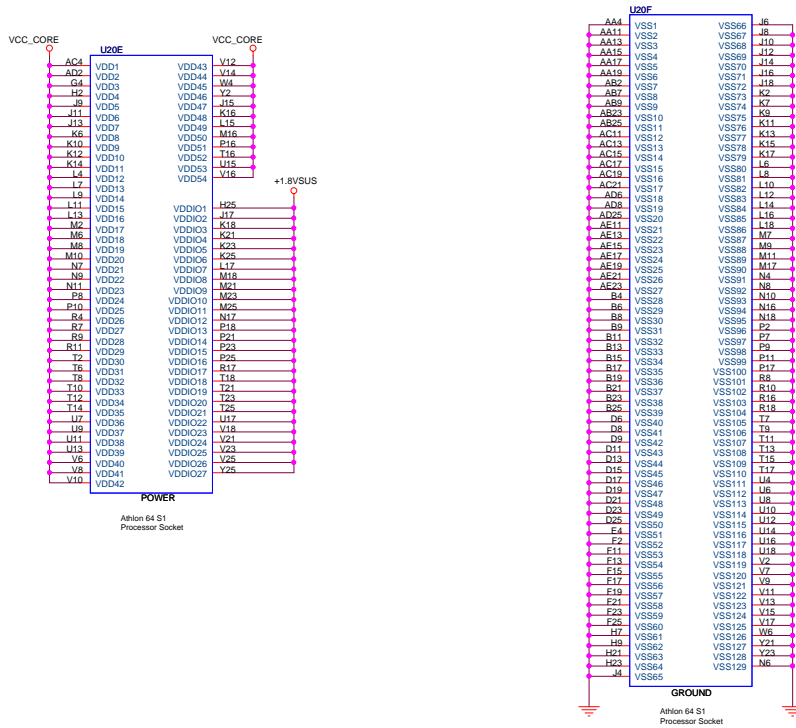
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS



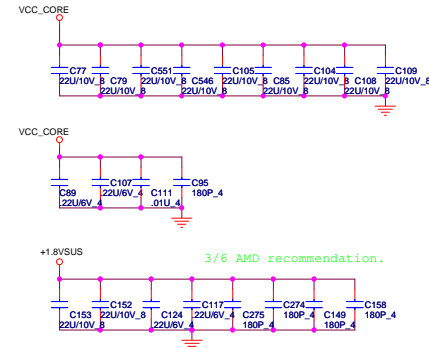
PROJECT :ZH3
Quanta Computer Inc.

ATHLON Control and Debug

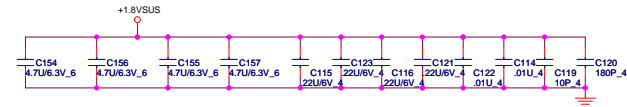




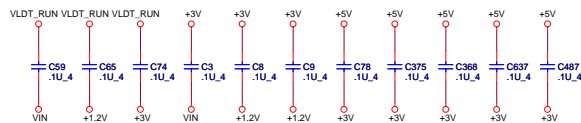
BOTTOMSIDE DECOUPLING



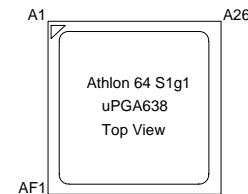
DECOUPLING BETWEEN PROCESSOR AND DIMMs PLACE CLOSE TO PROCESSOR AS POSSIBLE



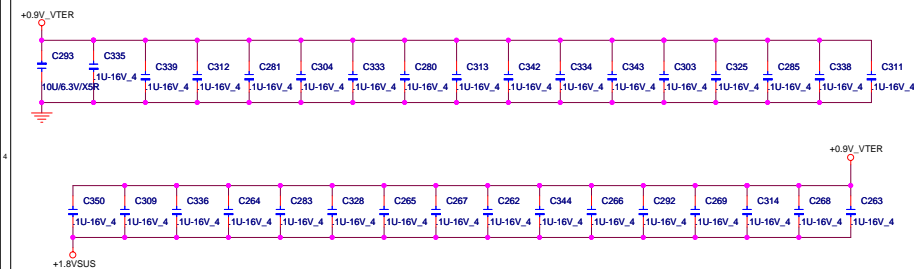
PROCESSOR POWER AND GROUND



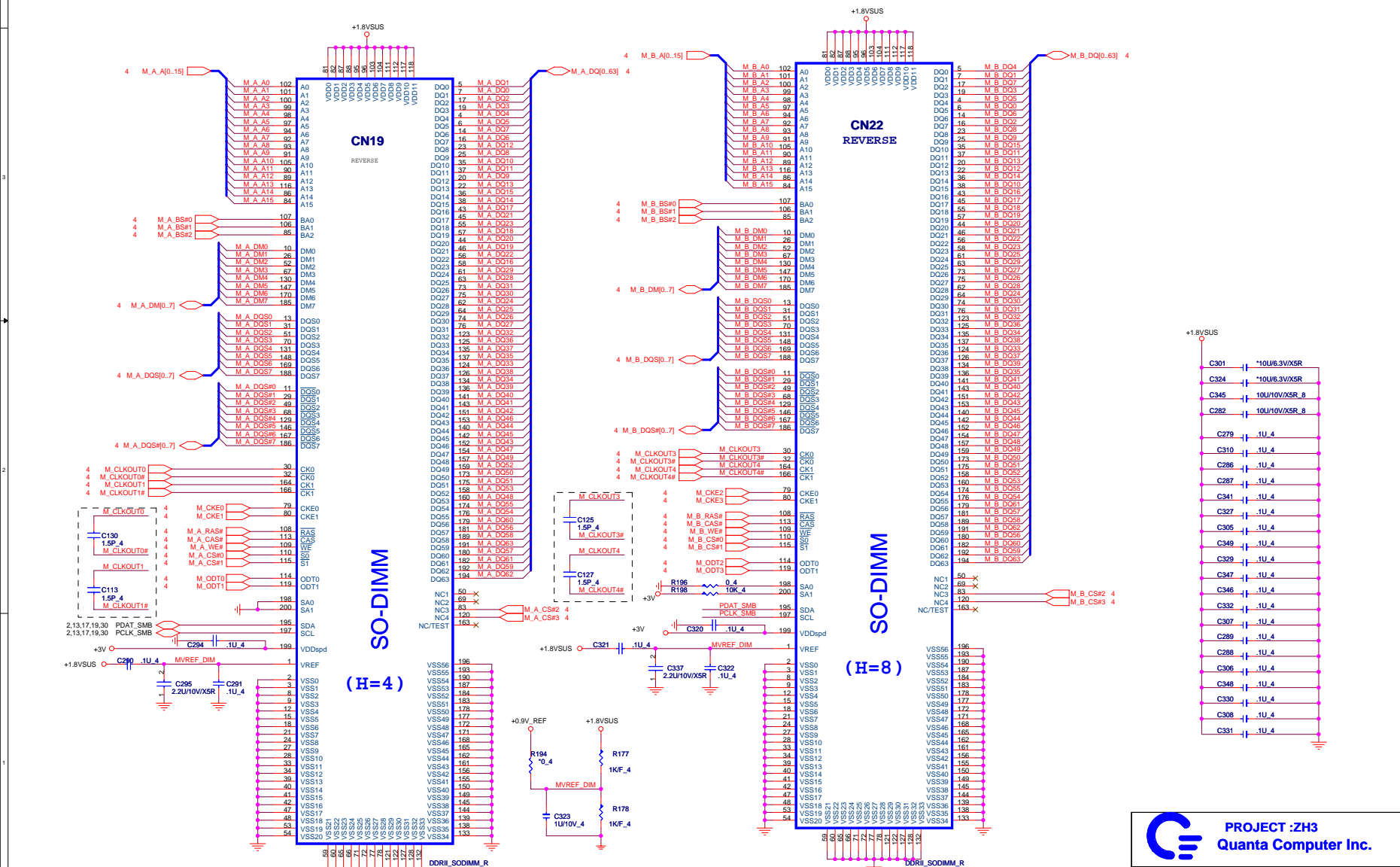
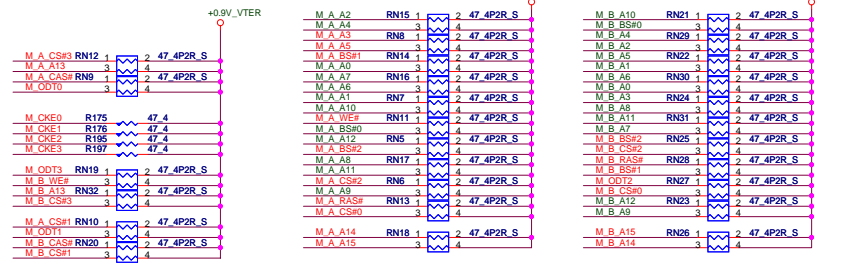
3/6 :ADD 0.1u CAPACITOR TO CROSS POWER PLANE.

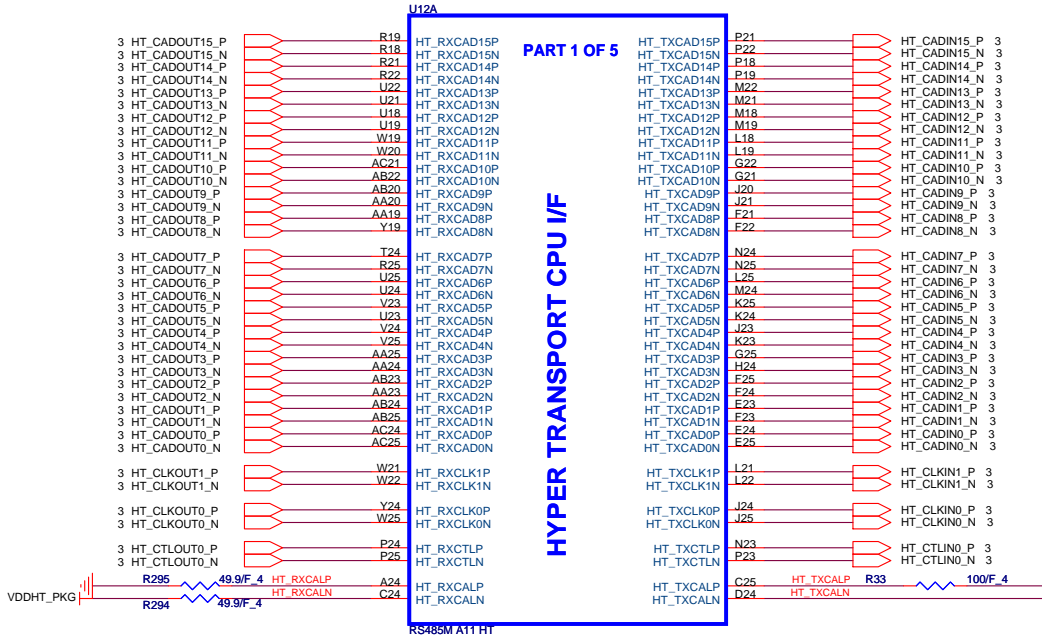


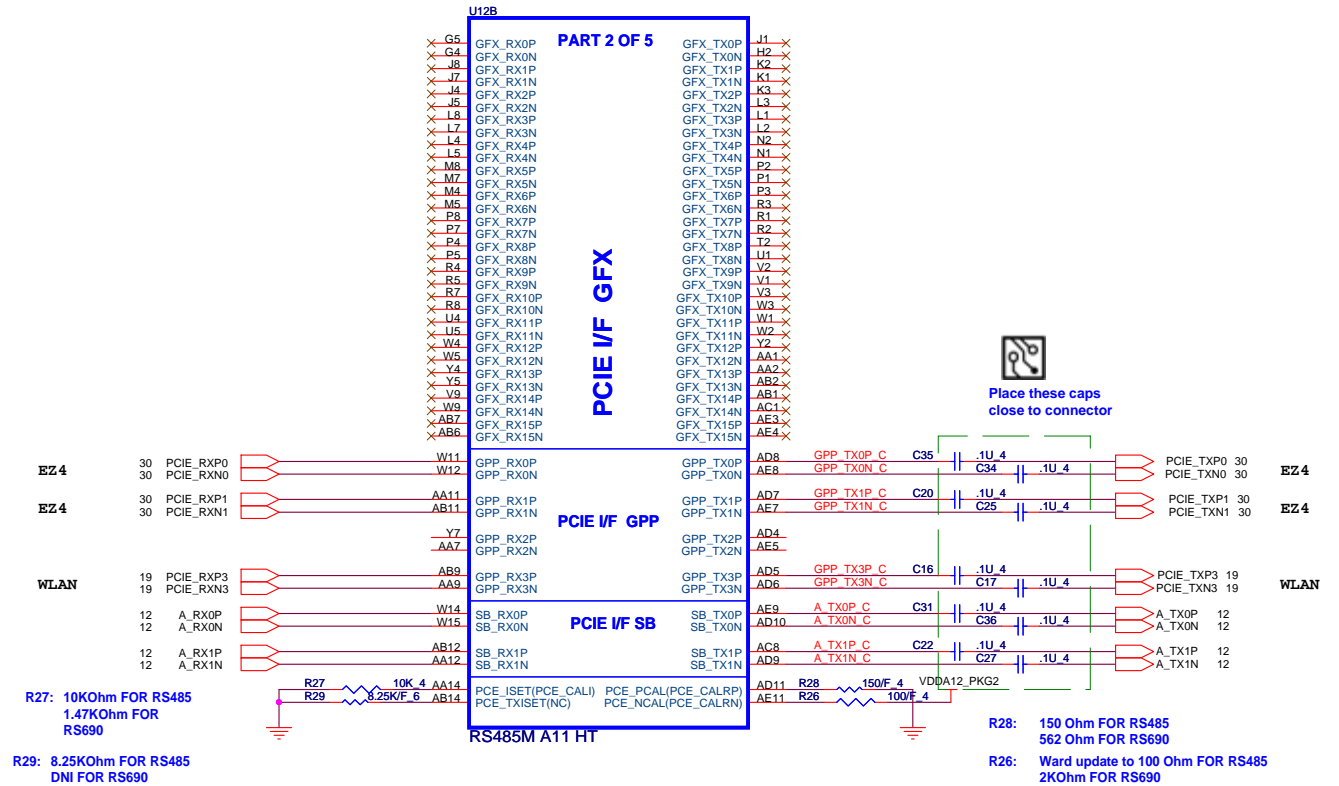
TERMINATOR DECOUPLING CAPACITOR

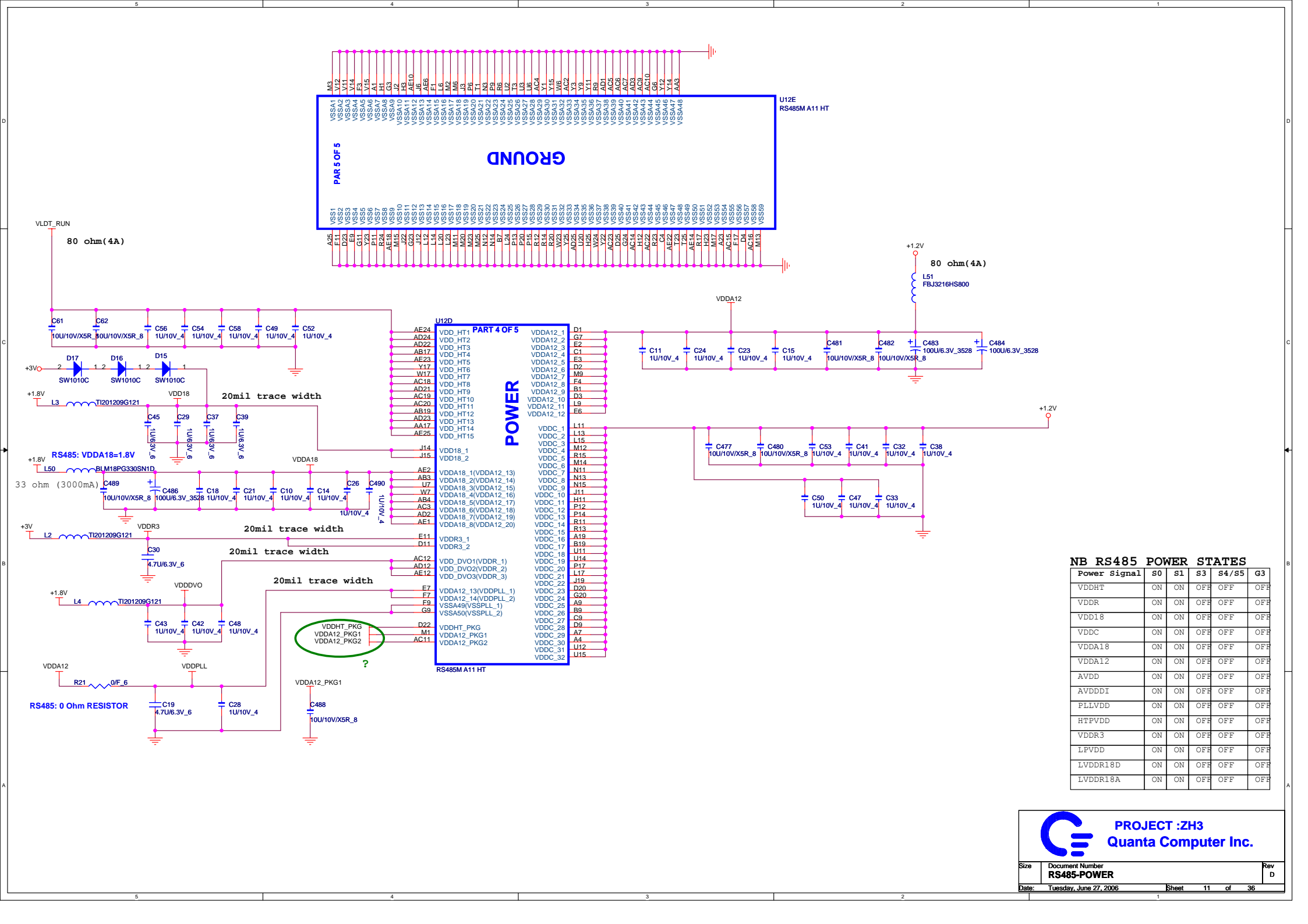


DDR2 TERMINATOR



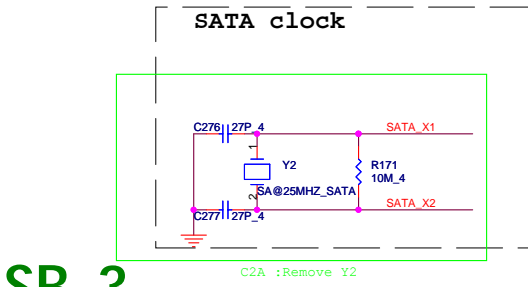
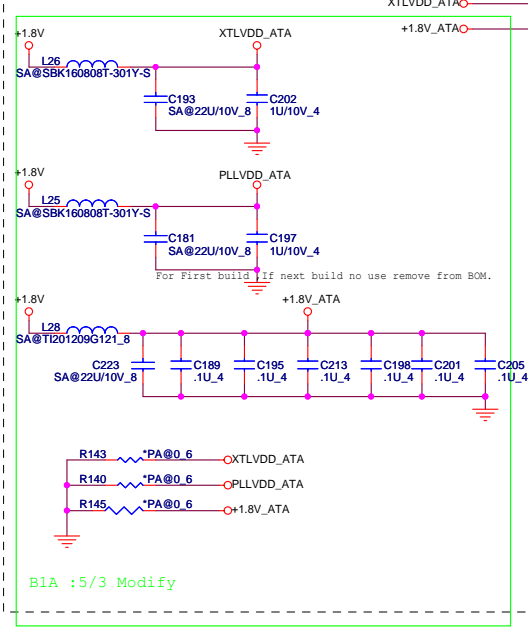






SB-3

SATA Power



C2A :Remove Y2

SB460 SB 27x27mm

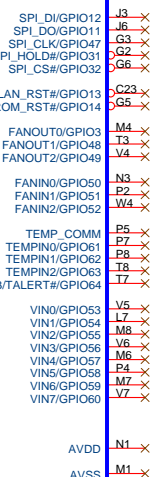
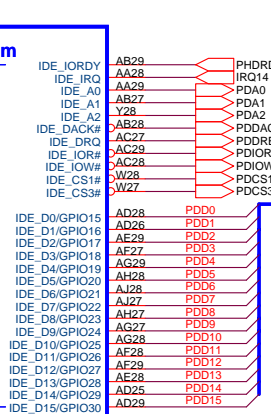
Part 2 of 4

SERIAL ATA

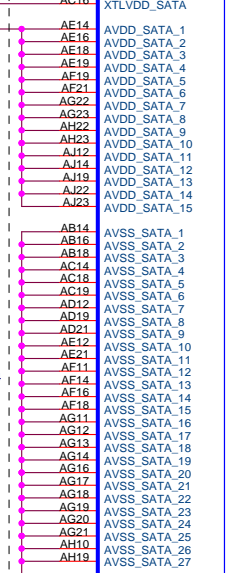
ATA 66/100

SPI ROM

HW MONITOR



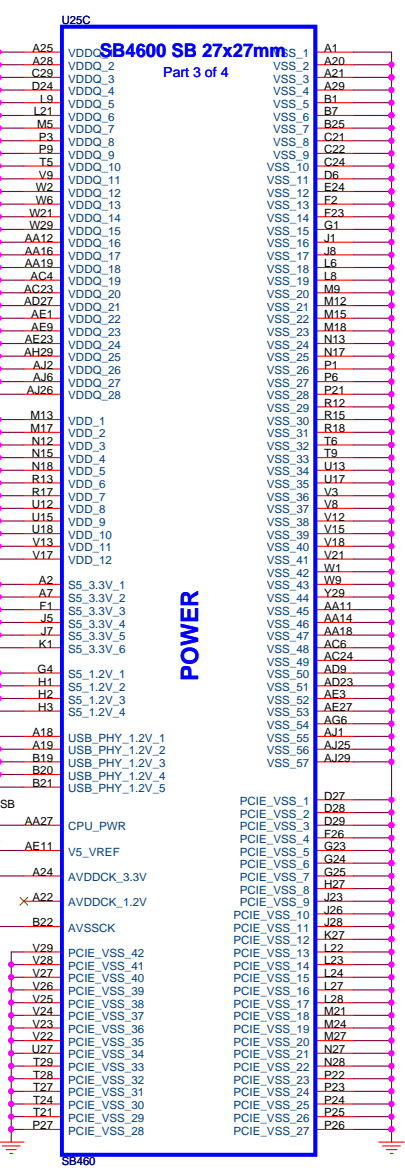
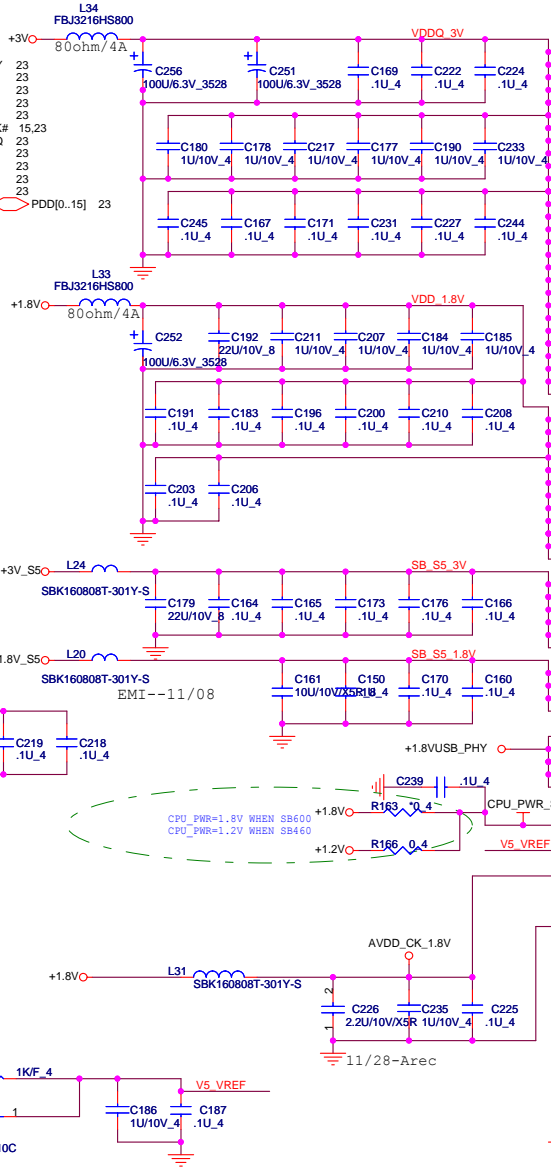
SERIAL ATA POWER



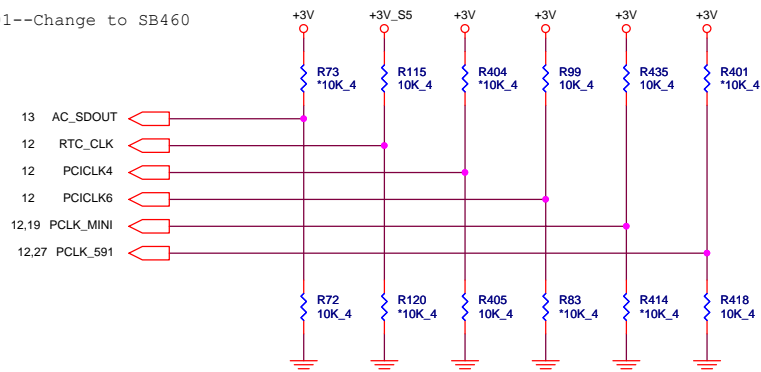
SB4600 SB 27x27mm

Part 3 of 4

POWER

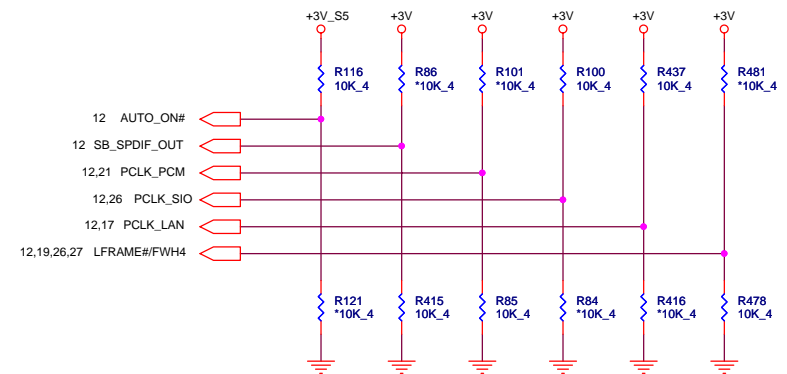


Size	Document Number	Rev
	SB450M HDD/POWER/DECOUPLING	D
Date:	Tuesday, June 27, 2006	Sheet 14 of 36

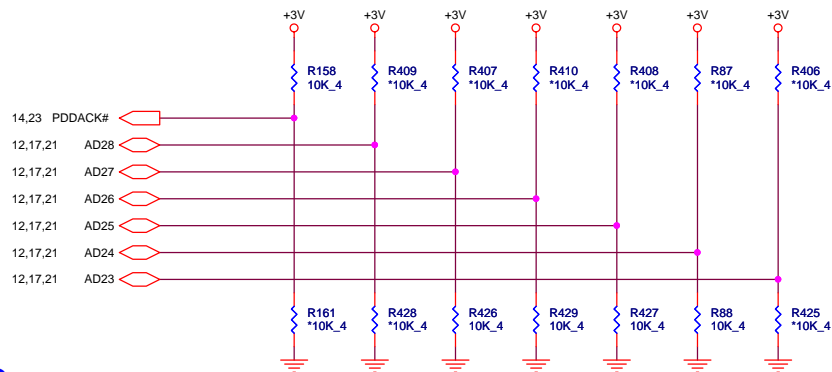


REQUIRED STRAPS

					PCLK_MINI	PCLK_591
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4 DEFAULT	L, L = FWH ROM NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]	



	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH BIOS ENABLE AFTER STARTUP	DISABLE THERMTRIP#



DEBUG STRAPS

	PDDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

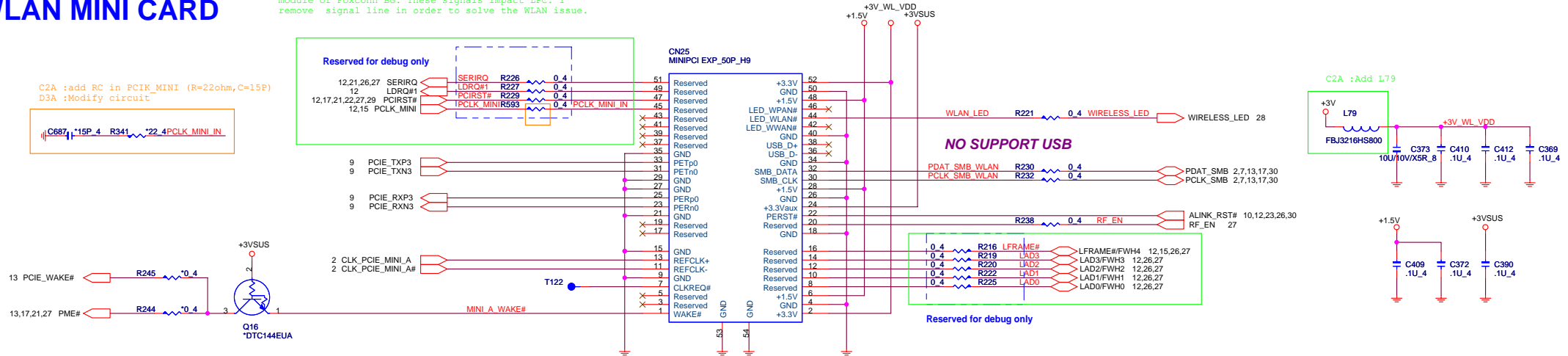


PROJECT :ZH3
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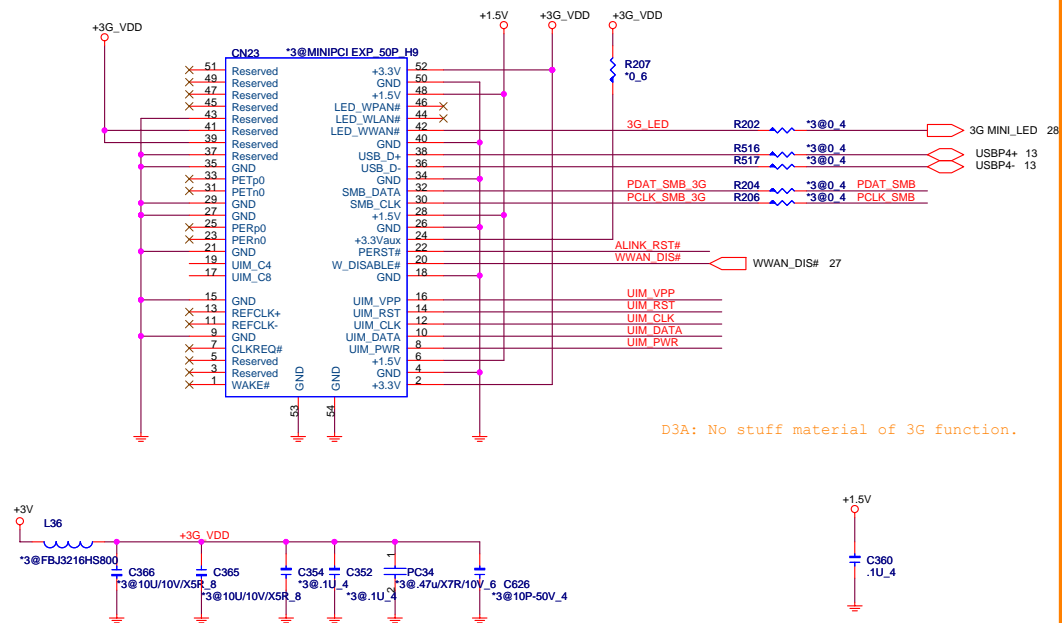
Size	Document Number SB460M STRAPS	Rev D
Date:	Tuesday, June 27, 2006	Sheet 15 of 36

WLAN MINI CARD

BLA:These signals of reserve have be used by wileless module of Foxconn BG. These signals impact LPC. I remove signal line in order to solve the WLAN issue.

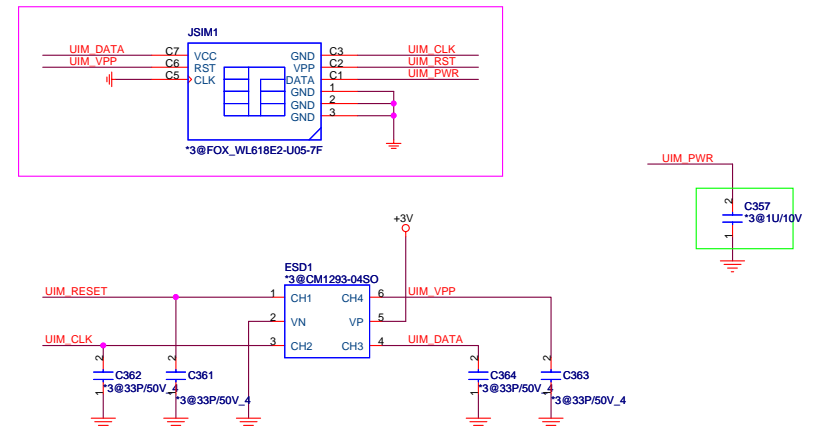


3G MINI CARD

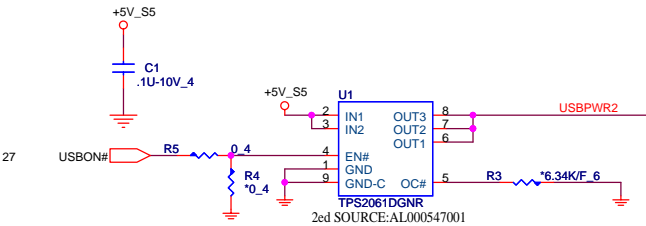
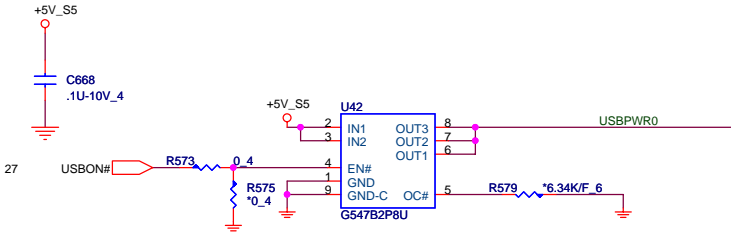


SIM CARD

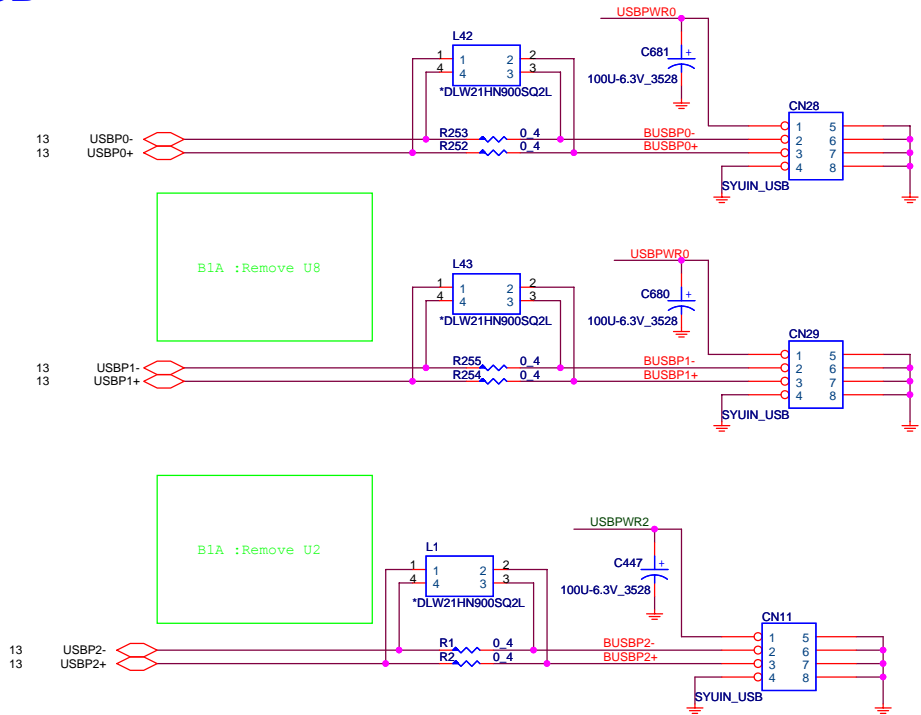
B1A: Change footprint
C2A: Change footprint & modify SIM card PIN define



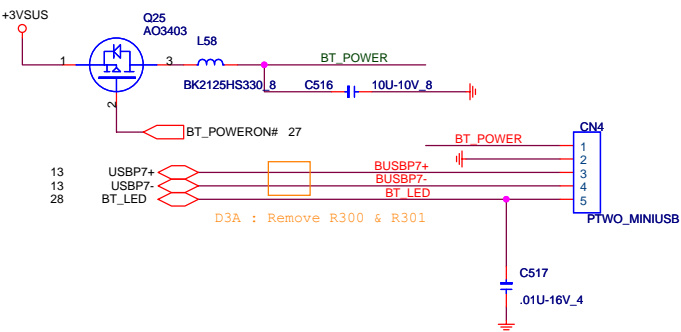
USB POWER SUPPLY

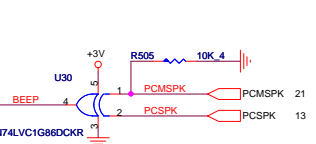
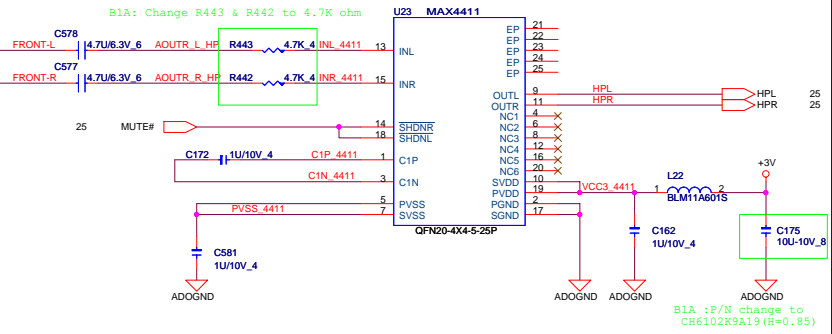
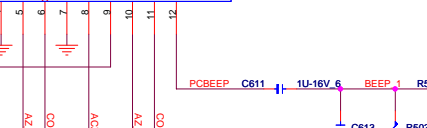
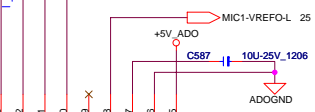
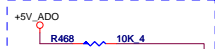
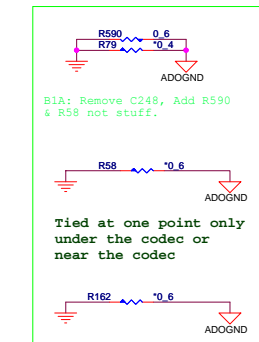


USB



BLUETOOTH MODULE CONNECTOR



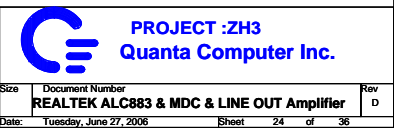


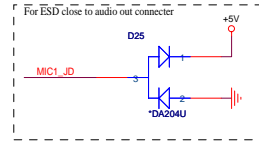
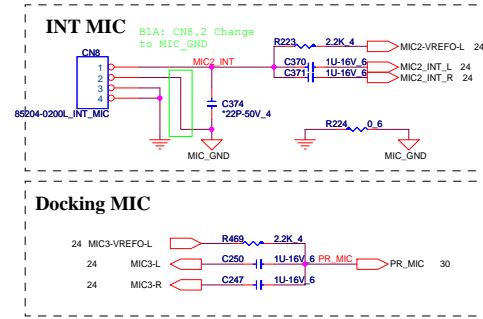
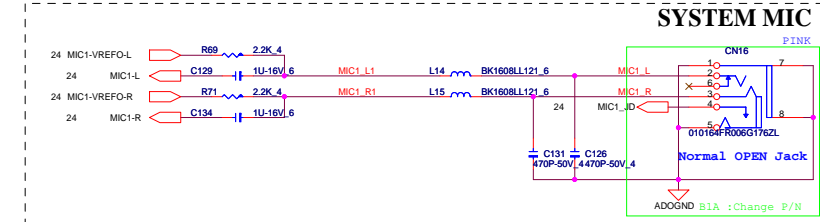
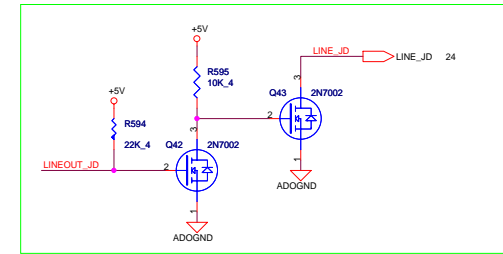
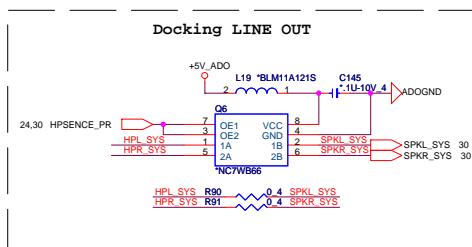
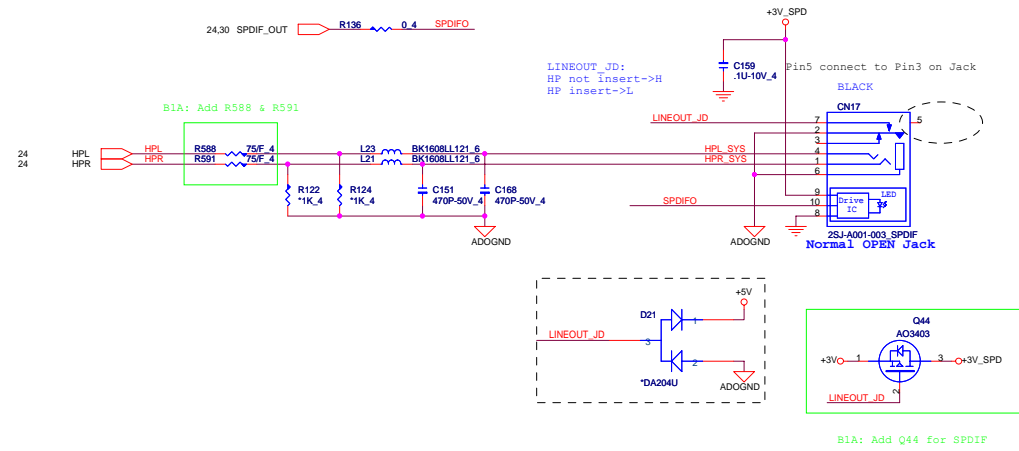
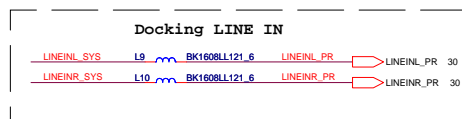
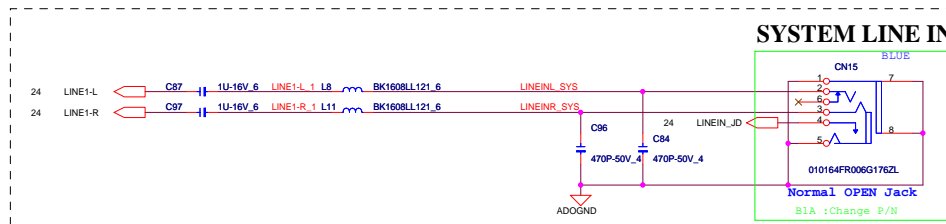
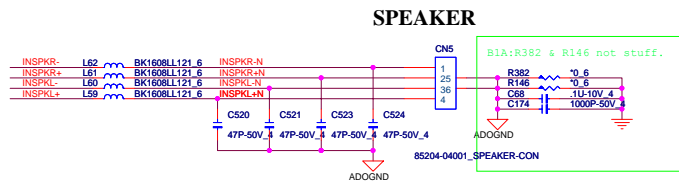
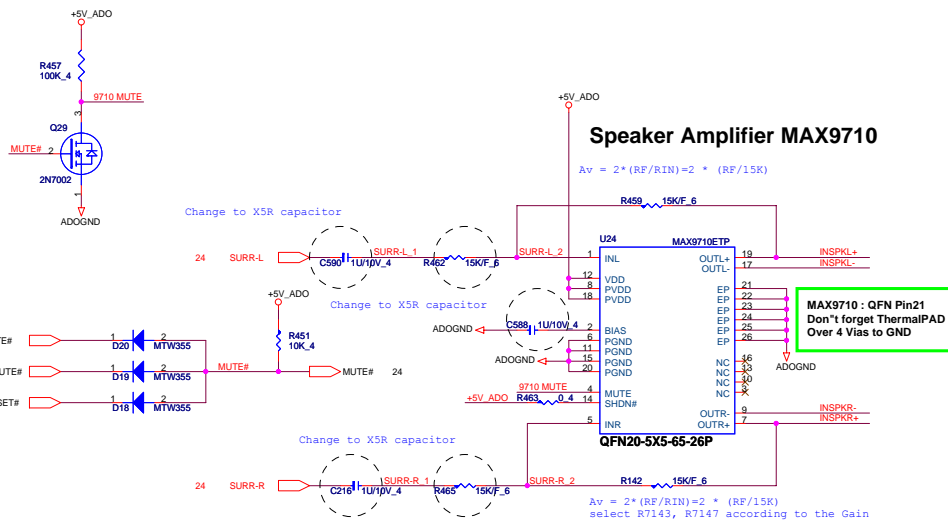
The schematic diagram shows the CN24 connector with the following connections:

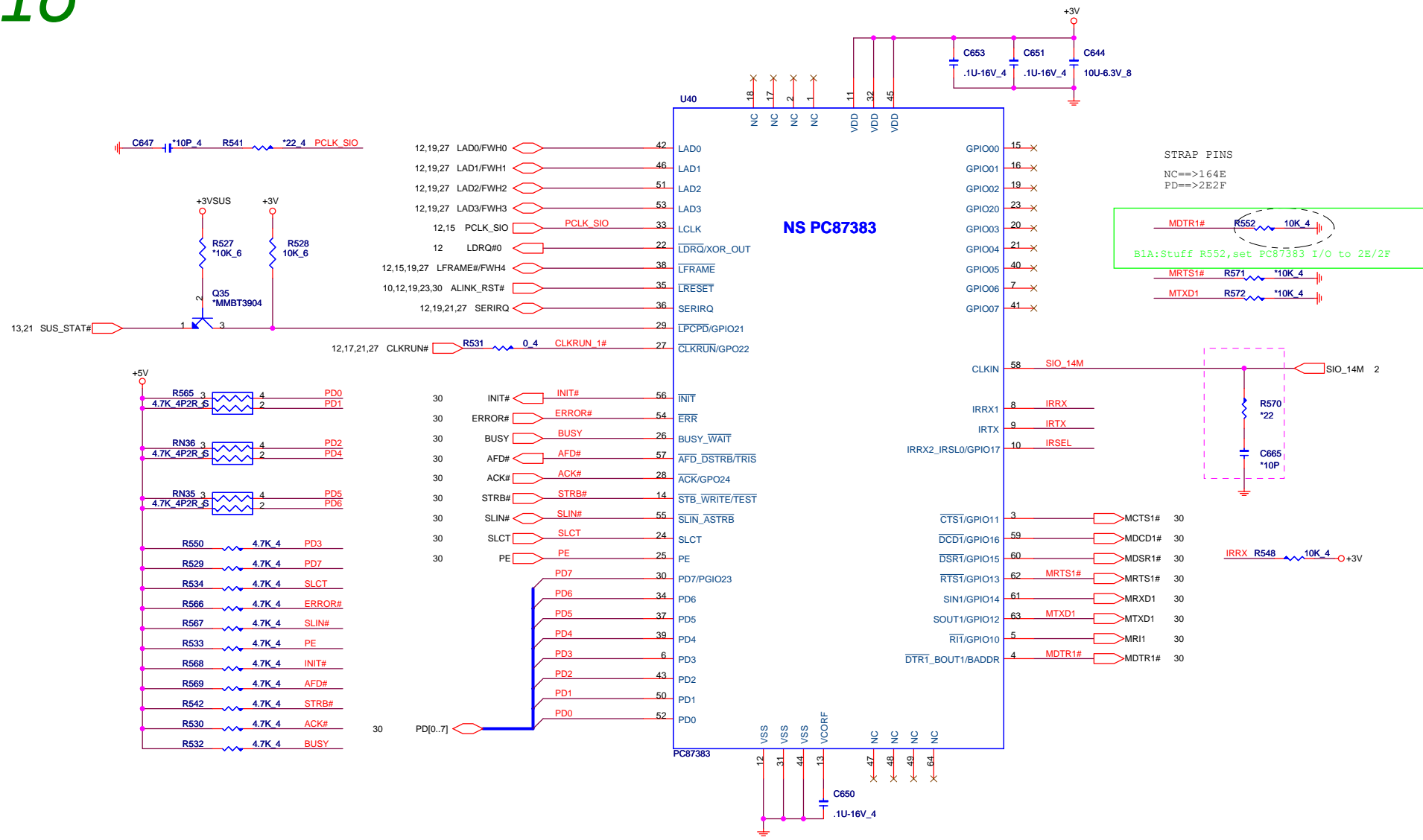
- Pin 1:** GND
- Pin 3:** AC_SDO
- Pin 5:** AC_SYNC
- Pin 7:** AC_SDI
- Pin 9:** AC_RST#
- Pin 11:** AC_BCLK
- Pin 12:** MDC

External components and connections include:

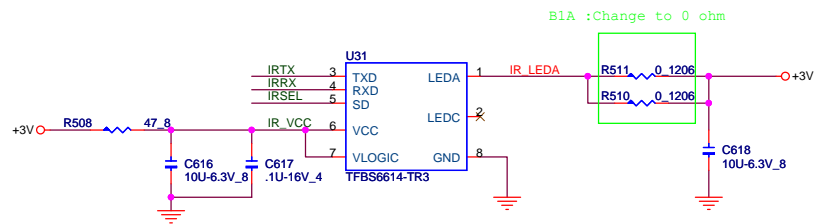
- Capacitor C629:** 10µF-10V_4, connected to pin 12 and ground.
- Capacitor C630:** 10µF-50V_4, connected to pin 12 and ground.
- Resistor R525:** 22_4, connected to pin 12 and ground.
- Capacitor C636:** 10µF-50V_4, connected to pin 11 and ground.
- Resistor R526:** 22_4, connected to pin 11 and ground.
- Signal Lines:**
 - CD_SDOUTA_MDC (Pin 3)
 - CD_SYNC_MDC (Pin 5)
 - CD_SDINO (Pin 7)
 - CD_RESET#_MDC (Pin 9)
 - CD_BITCLKA_MDC (Pin 11)

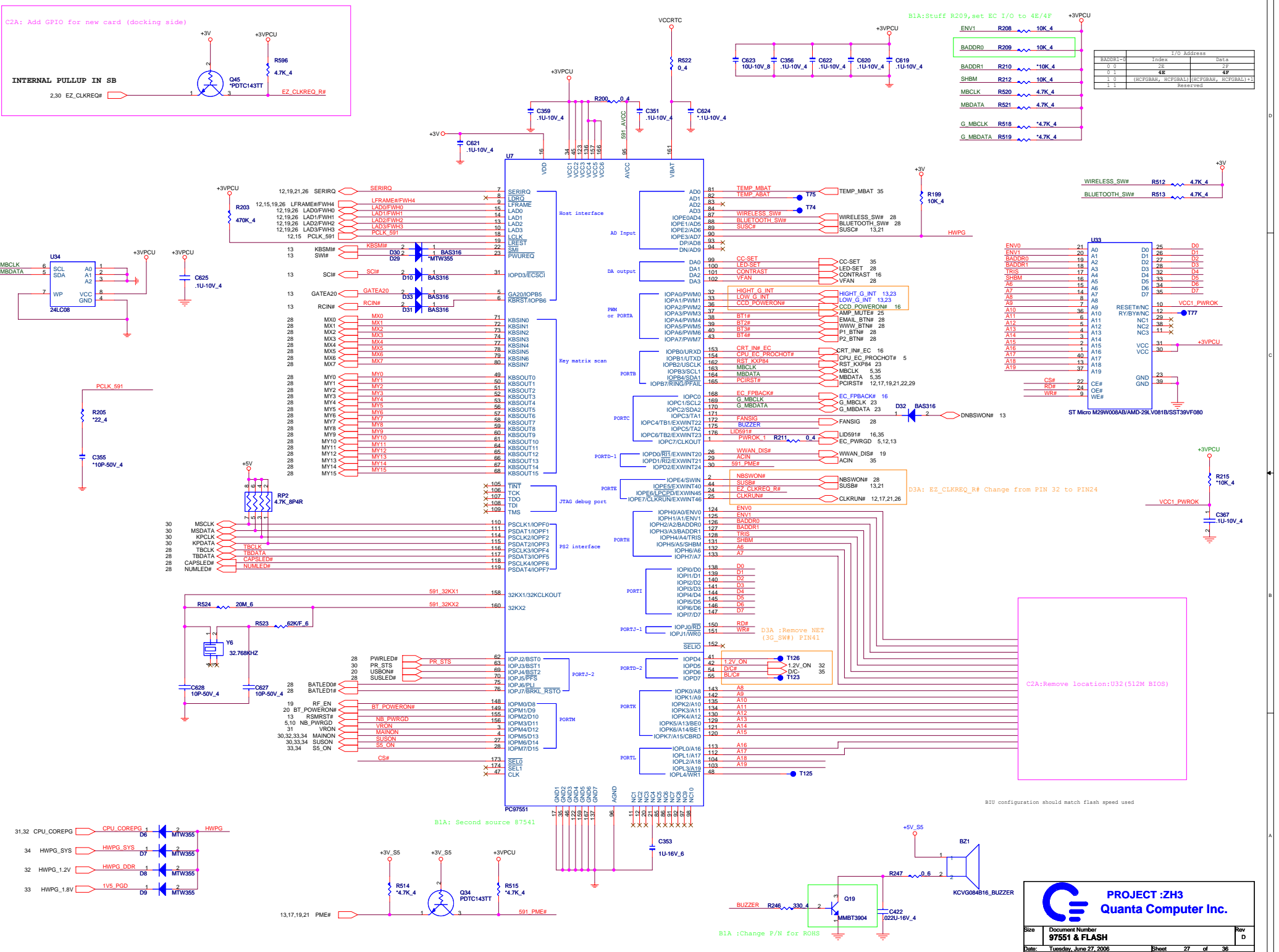


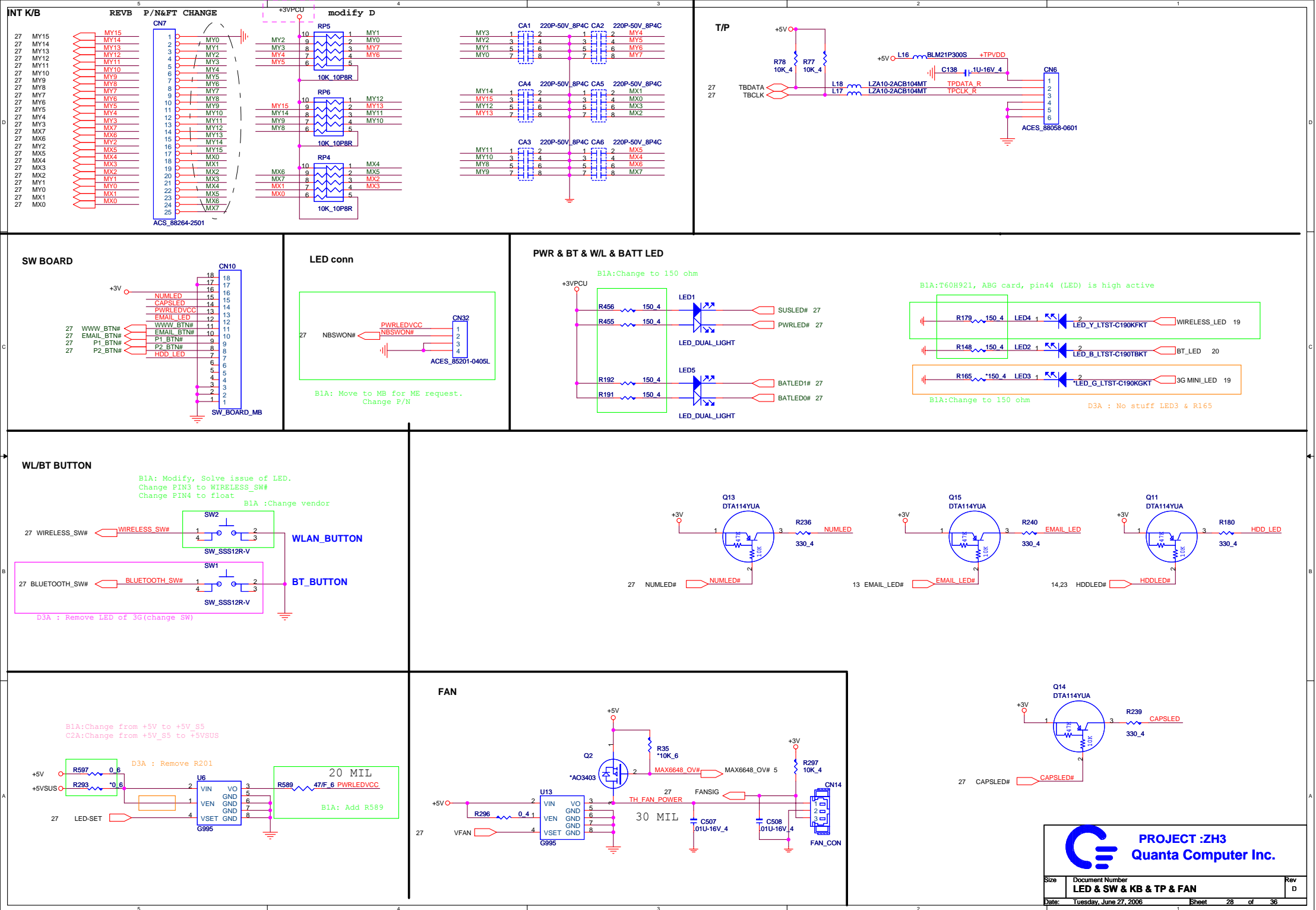


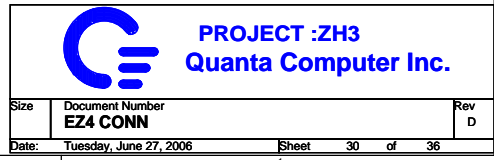


FIR

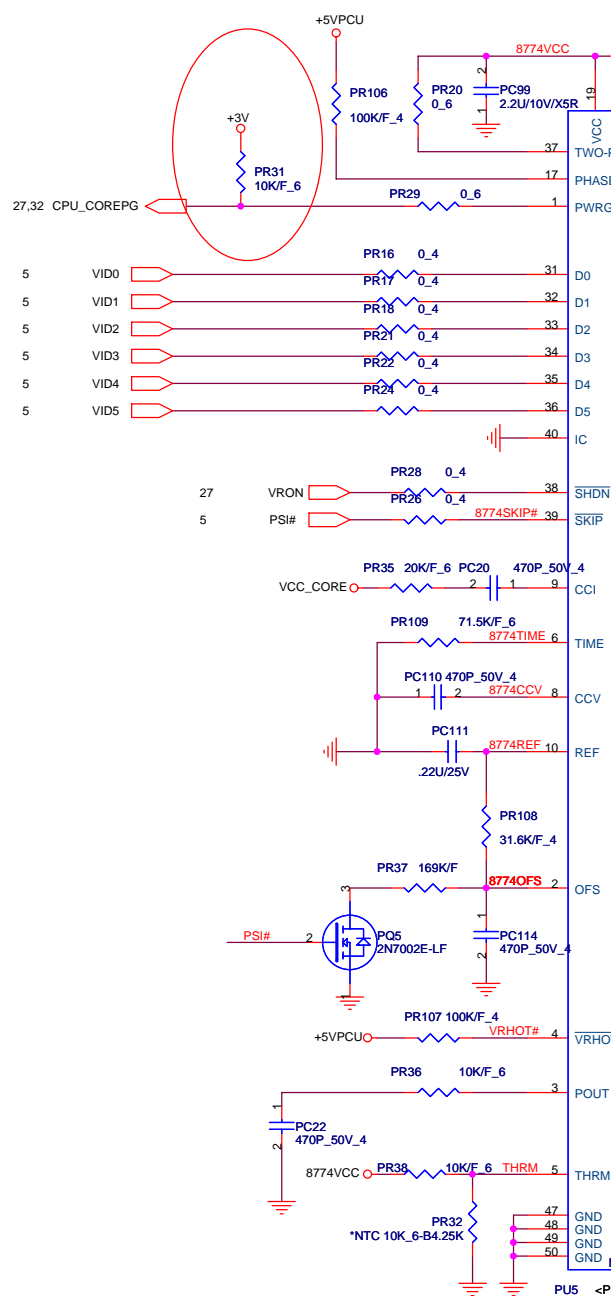




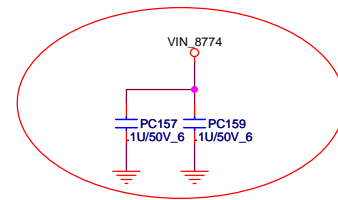
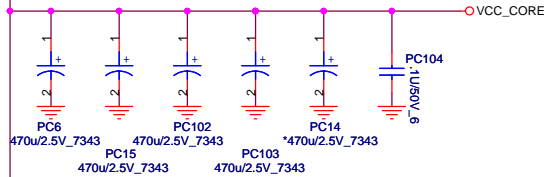
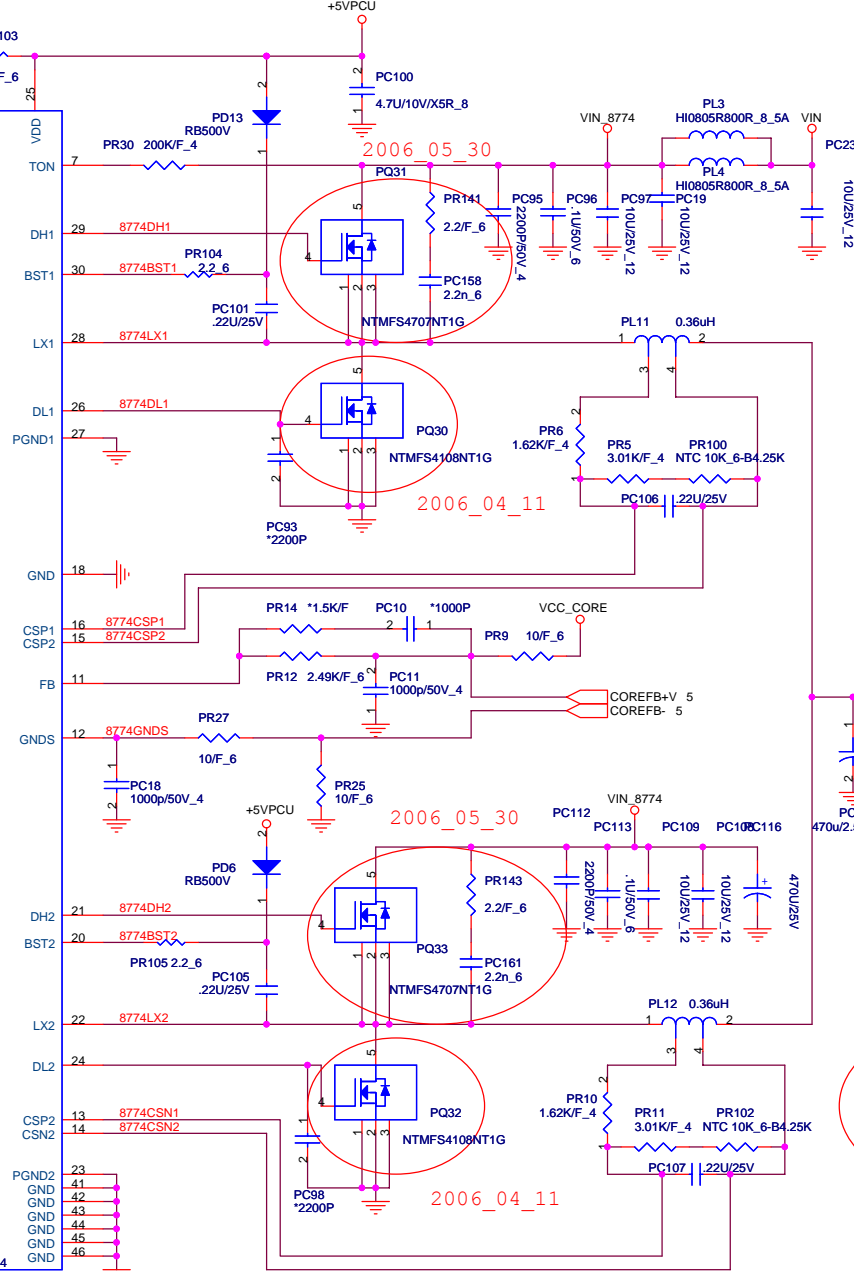




2006_03_06 for AMD



PUS <Pin Numbers Visible>
B1A:PUS Change footprint to -50P



2006-0417
For EMI

C2A :Modify to EC control ,
Remove PR66, Stuff PR65

27 1.2V_ON PR65 0.6
27,31 CPU_COREPG PR66 *10K/F 6

27 HWPG_1.2V PR53 0.6
PR52 10K/F_6
+3V

PC36 .1U/50V_6
PC39 1000p/50V_4
PR51 10K/F_6

D3A :Remove PC40, Add PR51

PU2 SC470ITSTRT
EN/PSV 14
VIN 13
VOUT 12
VCCA 11
FBK 10
PGOOD 9
GND 8

BST 14
DH 13
LX 12
ILIM 11
VDDP 10
DL 9
PGND 8

PC35 *.1u/25V_6
PC37 4.7U/6.3V_6
PC38 .1U/50V_6
PR58 15K/F_6
DH-1.2V
DL-1.2V

PQ20 FDS6612A
PQ21 FDS6690AS

VIN-1.2V
PL5 HI0805R800R_8_5A
PC45 .1U/50V_6
PC44 10U/25V_12
PC43 10U/25V_12

PL6 1.5uH-MSCDR1-104R
PC48 470u/2.5V_7343
PC51 470u/2.5V_7343
PC47 10U/6.3V_6

PR63 14K/F_6
PR59 10K/F_6
PC41 100p/50V_4
1.2V FB

2006-04-18

$$VOUT = (1 + R2/R3) * 0.5$$

27,30,33,34 MAINON MAINON PR48 0.6

PC129 .1U/50V_6
PC128 10U/10V/X5R_8
PC32 .1U/50V_6
+1.8V

PU7 SC4215
NC0 5
EN 6
VIN 8
NC1 9
ADJ 10
GND0 11
GND1 12

PC139 10U/10V/X5R_8
PC140 *150U/4V_3528
PC132 .1U/50V_6
R1 PR124 6.8K/F_6
R2 PR125 7.5K/F_6
1.5V-ADJ

$$Vo = 0.8 (R1 + R2) / R2$$

MAINON PR97
+3VPCU PR94
PU4 G923-330T1U
SHDN 1
GND 2
VIN 3
SET 4
PR95 20K/F_6
PR96 20K/F_6
PC88 10U/10V/X5R_8

$$Vout = 1.25(1 + R1/R2) = 1.25 (1 + 20K/20K) = 2.5V$$

PROJECT :ZH3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.2V & NBRUN	D
Date:	Tuesday, June 27, 2006	Sheet 32 of 36

change from NCP5214 to SC480IMLTRT



The schematic diagram illustrates the power supply section of the TMS320C6748 evaluation module. It features two main input lines: S5_ON and +3VPCU. The S5_ON line passes through a resistor PR33 (0.6 ohms) and a capacitor PC17 (47uF/10V/6) before entering the PU1 (G923-330T1U) voltage regulator at its SHDN pin. The +3VPCU line passes through a resistor PR34 (0.6 ohms) and enters the PU1 at its VIN pin. The PU1 regulator's GND pin is connected to ground, and its VO pin is connected to the +1.8V_S5 output. A feedback network consisting of resistors PR19 (47K) and PR23 (100K) is connected between the VO pin and the SET pin. The +1.8V output is also connected to a capacitor PC16 (10uF/10V/5R_8). A MOSFET PQ29 AO6402 is shown, with its gate connected to the +1.8V output through a resistor R55 (0.4 ohms) and a capacitor PC5 (47uF/10V/6). The MOSFET's source is connected to ground, and its drain is connected to the +1.8V output through a capacitor PC90 (0.1uF/50V/6). The +1.8V output is also connected to the +1.8VSUS input.

$$\begin{aligned} V_{out} &= 1.25(1+R_1/R_2) \\ &= 1.25(1+44K/100K) \\ &= 1.8V \end{aligned}$$

Change list

Item	Fixed Issue	Modify List	Schematic Rev.	PG#	
1	New card issue.	NC_EN# connect the PIN4 & PIN17 of CN2 and PIN11 & PIN12 of CN14	B	13,31	
2	New card issue.	Change from USB8 to USB5 for new card,	B	13,31	
3	Lan issue.	Signal change from INTF to INTG	B	12,17	
4	INT MIC issue.	CN8.2 change from MIC2_INT to MIC_GND	B	25	
5	Wireless LED issue.	SW2.1 change from GND to wireless_sw#, SW2.2 change from wireless_sw# to GND.PIN3,4 is float	B	28	
6	DVI issue	Q40.1 change from PHL_DATA to DDC_DATA	B	29,30	
7	RAMP test				
8					
9					
10					
1					
2					
3					
4					
5					
6					
7					
8					
1					
2					
3					